

REMARKS

Applicant respectfully requests reconsideration. Claims 1-26 were previously pending in this application. New claims 27-38 have been added. As a result, claims 1-38 are pending for examination. No new matter has been added.

Rejections Under 35 U.S.C. §102

The Examiner has rejected claims 1, 3-5, 7, 10-14, 20-22 and 25-26 under 35 U.S.C. §102(e) as being anticipated by U.S. Patent No. 6,879,139 (Brown). Reconsideration is requested.

Upon closer inspection, it will be seen that the structure and operation of Brown and that of the present invention are significantly different and that the subject matter of the rejected claims is novel over Brown.

Without intending to affect the construction of the claims and without adding to or subtracting from the disclosure, it will be observed that the inventive subject matter relates to a controller in which a single state machine (see claim 1, for example) can control multiple power supplies, the power supplies not being part of the claims. The state machine has an input portion, which in the examples given in the specification includes a fault monitor (shown in Figure 3), a sequence detector (Figure 5) and a timer (Figure 6) which can be used to force a transition from one state to the next if the tested event does not occur in a reasonable time period (some of the foregoing not reflected in claim 1). In use, the state machine progresses from one predefined state to the next depending on which event causes a state transition to occur. At each transition new control words are written to a mask controlling operation of the fault monitor, sequence detector and timer such that the same piece of hardware is used to check for different conditions in different states at different times because a new (state dependent) control mask is loaded at each transition. Referring to the language of claim 1, this is expressed as "the operation of the logic core is modified upon a transition from a state to a succeeding state in accordance with data held in the memory."

By contrast Brown seems to describe a system where a plurality of individual state machines CSM0 to CSM5 work to control their respective power supplies. There is no modification of the logic core upon state transitions.

Considering any individual state machine, it has shadow registers STREN(X), SHDNEN(X) and FLTEN(X) which set masks to monitor for conditions to be monitored as part of start up, shut down and fault conditions, respectively. The registers are loaded at power up but are *not altered thereafter*. Thus, for any single one of the state machines the operation of the logic core is not modified in accordance with data held in the memory as part of a transition from one state to the next. The individual state machines act in unison to form a composite state machine. However, even when one considers the composite state machine, one sees that its logic is not modified as a result of state transitions.

Further, the composite controller of Brown does not really form a single state machine, anyway, as at any given instant the state of the machine may be ill-determined. As shown in Figure 4, the state machines 40 and 42 act independently in response to a trigger signal and the sequence in which the power supplies 0 and 2 are energized may be determined *by propagation delays* within the state machine.

Consequently, none of claims 1-26 is anticipated by Brown and the rejection should be withdrawn.

Accordingly, withdrawal of this rejection is respectfully requested.

Rejections Under 35 U.S.C. §103

The Examiner has rejected claims 2, 6, 8, 9, 15-19 and 23-24 under 35 U.S.C. §103(a) as being unpatentable over Brown in view of U.S. Patent No. 3,626,427 (MacSorley). Reconsideration is requested.

As regards the suggestion that some of the claims would be obvious in view of a combination of Brown and MacSorely, this is unfounded. Claim 1 is novel over Brown as set forth above. The rejected claims all depend from claim 1, directly or indirectly. Hence, it would be necessary for the Examiner to find another basis for rejecting claim 1 before the dependent claims could be rejected on prior art grounds. The rejection is therefore moot.

Nevertheless, for completeness it is noted that the Examiner has rejected claims 6 and 23 on the basis that Brown assertedly teaches a controller which includes a mask for indicating whether a condition should be monitored. He further indicated the provision of an invert signal would be obvious from MacSorely (citing col. 28 lines 35 to 50 and col. 48 lines 68 to 75). The Examiner is mistaken because of the facts that: 1. In Brown, the state machines transmit state data between themselves and any signal conditioning that would have needed to be done would be performed by the ISM (input state machine); and 2. Col. 28 lines 35 to 50 in context, i.e. lines 35 to 69, actually relates to a signal blocking circuit. The other passage referred to by the Examiner (col.48) is a circuit for detecting a key depression. Surely the person ordinarily skilled in the art would not consider this to be relevant.

We need not even consider whether the Examiner has established a proper motivation for combining the references. If they were combined, the claimed invention surely would not be the result as MacSorely does not supply the teachings absent from Brown and discussed above.

Accordingly, this rejection should be withdrawn.

New Claims

Claims 27-38 are added to claim additional aspects not previously claimed.


CONCLUSION

A Notice of Allowance is respectfully requested. The Examiner is requested to call the undersigned at the telephone number listed below if this communication does not place the case in condition for allowance.

If this response is not considered timely filed and if a request for an extension of time is otherwise absent, Applicant hereby requests any necessary extension of time. If there is a fee occasioned by this response, including an extension fee, that is not covered by an enclosed check, please charge any deficiency to Deposit Account No. 23/2825.

Respectfully submitted,
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